METHOD OF REDUCING POLYSILICON DEPLETION IN A POLYSILICON GATE ELECTRODE BY DEPOSITING POLYSILICON OF VARYING GRAIN SIZE

ABSTRACT OF THE DISCLOSURE

Polysilicon electrical depletion in a polysilicon gate electrode is reduced by depositing the polysilicon under controlled conditions so as to vary the crystal grain size through the thickness of the polysilicon. The resulting structure may have two or more depth-wise contiguous regions of respective crystalline grain size, and the selection of grain size is directed to maximize dopant activation in the polysilicon near the gate dielectric, and to tailor the resistance of the polysilicon above that first region and more distant from the gate dielectric. This method, and the resulting structure, are advantageously employed in forming FETs, and doped polysilicon resistors.